CAT874 Hardware Manual

SILICON LINUX CORPORATION
シリコンリナックス株式会社

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Table of contetns 目次

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Operationusing Linux

```
$: This symbol indicates that a general user ( “kaihatsu” on this machine) operates it.
#: This symbol indicates that need to operate by root user. If you are using “kaihatsu” user to log in
 use su command.
\: Backslash is ￥ mark on Japanese keyboard and font. Please enter backslash if your using English base
d system.
```

この文書の書式について

```
$ 記号は一般ユーザ（本機では kaihatsu ）で操作することを示します。
# 記号は root ユーザで操作することを示します。一般ユーザからは su コマンドで root ユーザに変わること
\ バックスラッシュは日本語キーボードで ￥マークです。\ は￥を入力してください。
```

Other basic conditions

```
Development PC：PC used for development. Mainly means Linux installed on VirtualBox.
Target board:：In this document, CAT874 Linux board.
```

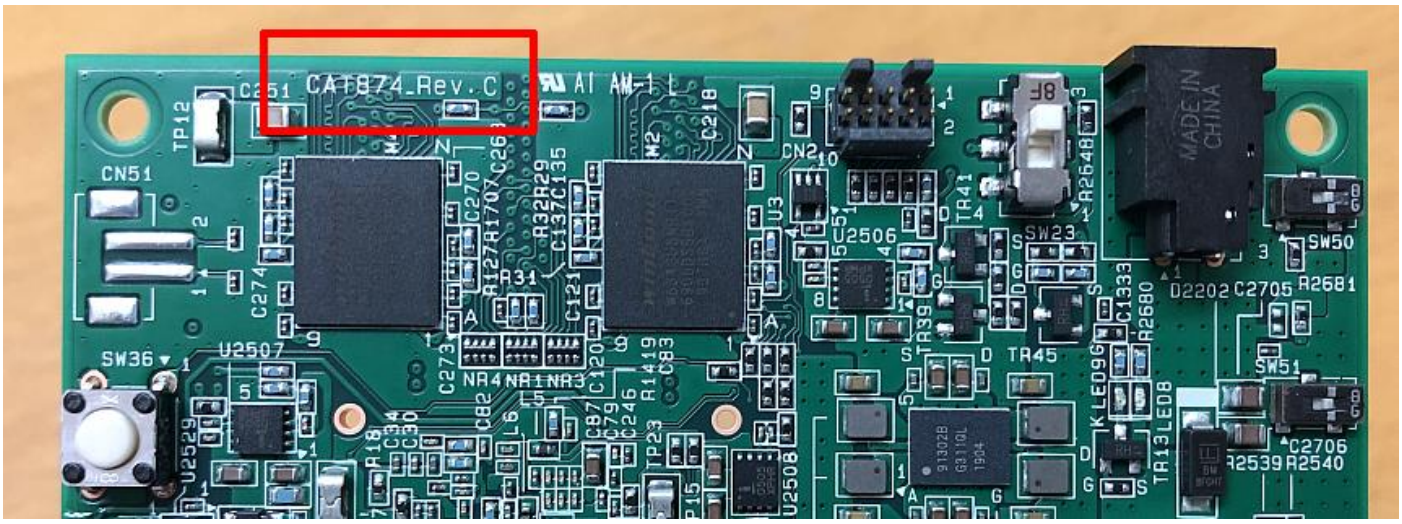
```
開発 PC：開発に使用するパソコン。主に VirtualBox にインストールされた Linux を意味します。
ターゲットボード：本書では CAT874 Linux ボードを意味します。
```

Reversion History of this document 改版履歴

July 5. 2019.	Initial Release. 初版
August 26. 2019	Correct some typo errors. 誤字修正
Jan. 20. 2020	Add CAT874 Rev.C CAT874 Rev.C 基板について追記
Jan. 12. 2022	Add CAT874 Rev,E CAT874 Rev.E 基板について追記
Mar. 22. 2023	Fixed SW50, SW51 CJS-1200TA Image picture
Non. 20. 2023	注意書き追加.　Added Notice

1 Reversion History of board 基板改版履歴

1.1 CAT874 Main board



Rev.A	2018-12-13	Not provided. 1st Trial production.
Rev.B	2019-04-19	Not provided. 2nd trial production.
Rev.C	2019-11-07	Fix Reverse connection UART0(CTS/RTS,TXD/RXD) and UART1(TXD/RXD) UART0(CTS/RTS,TXD/RXD)がテレコ修正、 UART1(TXD/RXD)がテレコ修正 CN2 (JTAG) PRESETn_18 (input) 修正 (Fix) Wi-Fi Bluetooth ANT chip (Change) MBKPRST_N voltage change (Fix) CN2 JTAG TRSTn add pull-up or pull-down register, open-switch (Optimize) SW50, SW51 CPU fan is abolished. CPU ファン廃止 for details. see “CAT874_RevC_Changes_20200120.docx” 詳細は “CAT874_RevC_Changes_20200120.docx”
Rev.D	2020-10-13	Not provided. Trial production for Rev.E version.
Rev.E	2020-11-10	eMMC / USB2.0 OTG Version Added eMMC Added USB2.0 OTG Added USB3.0 Type-A Remove USB3.0 type-C Remove 96 Low Speed Connector PCM_FS, PCM_CLK, PCM_DO, PCM_DI Remove 96 High Speed Connector MIPI-DSI out Remove 96 High Speed Connector SD I/F

		Remove 96 High Speed Connector USB I/F for details. see “CAT874_RevE_Changes_20210112.docx” 詳細は “CAT874_RevE_Changes_20210112.docx”

CAT874 Revision Differences

	Rev.A , Rev.B , Rev.C	**Rev.D , Rev.E**
eMMC	-	16GByte
USB3.0	Type-C x1	Type-A x1
USB2.0	Type-A	microB OTG.
	Type-A	-
	96 boards High speed con.	-
	Sub-board for TouchScreen	-
HDMI	TDA19988BET	ADV7513BSWZ
MIPI-DSI	4 lanes	-
96 Low Speed Connector	Alternate Sound PCM FS,CLK,DO,DI	-
96 High Speed Connector	Alternate SD Alternate USB	-

1.2 CAT875 (Sub board)

Rev.A	2018-12-13	1st production

2　Hardware specifications summary ハードウェア仕様概要

Rev.A,　Rev.B,　Rev.C

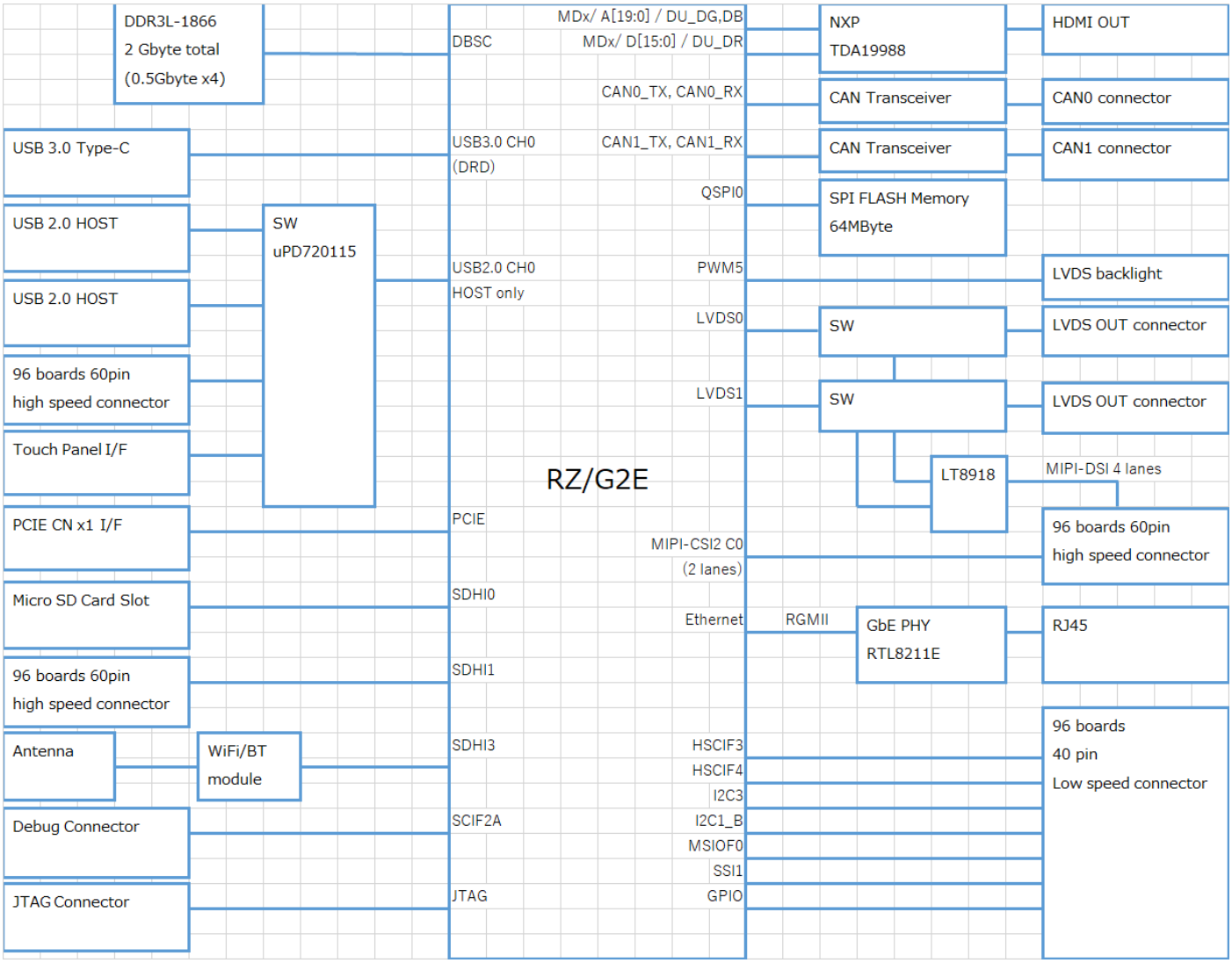
```
CPU               Renesas Electronics RZ/G2E  Dual Cortex®-A53
CLOCK             CPU Clock 1.2GHz
Main Memory       DDR3L-1866 x32bit 2GByte
QSPI-NOR-FLASH    64MByte

POWER             DC 12V

Interfaces
    GigaBitEthernet x1
    DigitalVIDEO  HDMI compatible x1
                  MIPI-DSI x1
                  LVDS dual channel x1
    USB  2.0 x2
    USB  3.0 Type-C x1
    MicroSD socket x1
    96boards Compatible Low speed connector, High speed connector
    Serial Console Connector  x1
    WiFi / Bluetooth
    CAN x2
    JTAG
```

Rev.D,　Rev.E

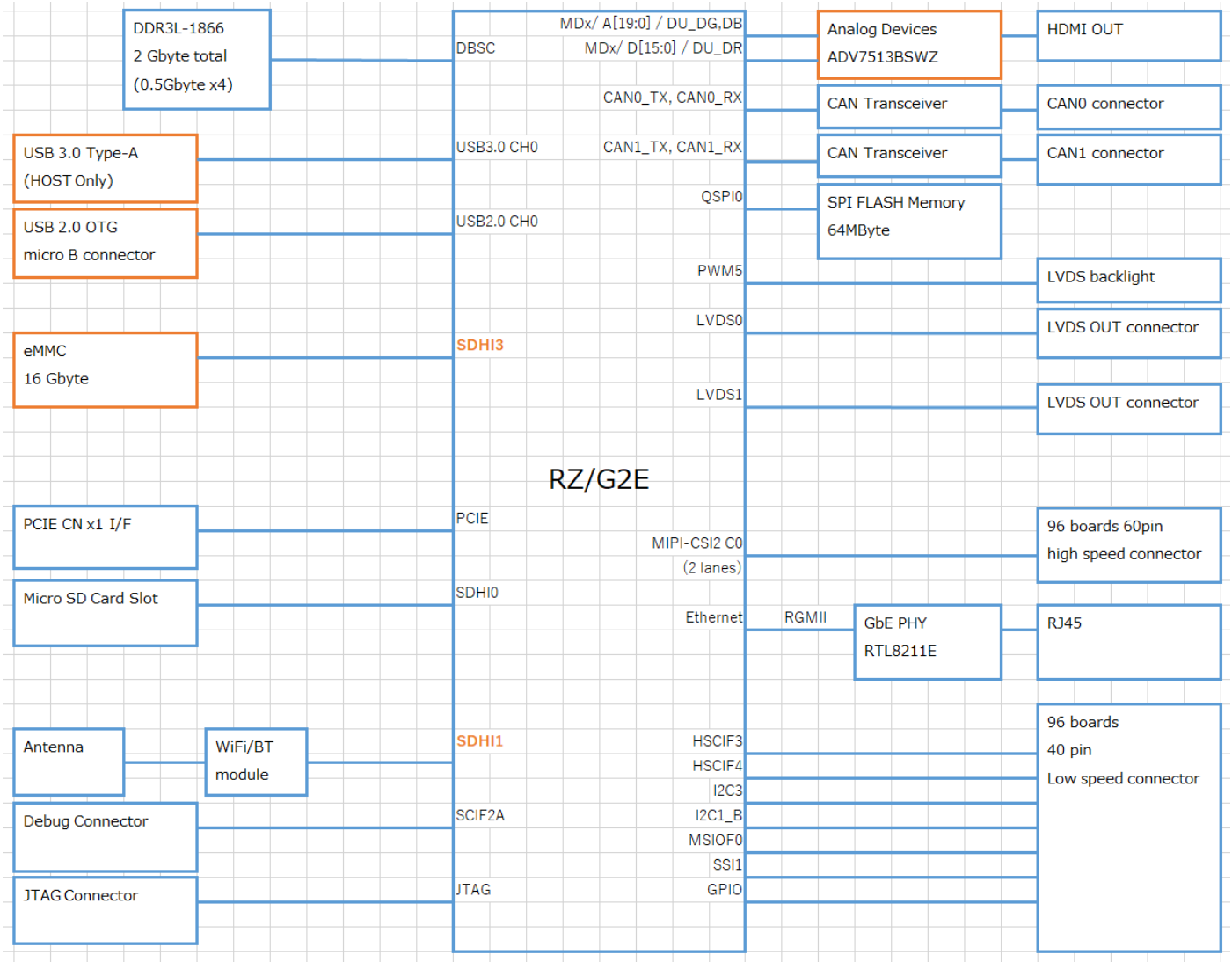
```
CPU               Renesas Electronics RZ/G2E  Dual Cortex®-A53
CLOCK             CPU Clock 1.2GHz
Main Memory       DDR3L-1866 x32bit 2GByte
QSPI-NOR-FLASH    64MByte

POWER             DC 12V

Interfaces
    GigaBitEthernet x1
    DigitalVIDEO  HDMI compatible x1
                  LVDS dual channel x1
    USB  2.0 OTG x1
    USB  3.0 Type-A x1
    MicroSD socket x1
    96boards Compatible Low speed connector, High speed connector
    Serial Console Connector  x1
    WiFi / Bluetooth
    CAN x2
    JTAG
```

3 Block diagram ブロック図

3.1 Rev.A, Rev.B, Rev.C



3.2 Rev.D, Rev.E



Add:

e-MMC 16Gbyte

Change:

USB 3.0 Type-C (DRD) to USB3.0 Type-A (Host Only)

USB 2.0 HOST x4 to USB 2.0 OTG x1

RGB to HDMI bridge LSI

Remove;

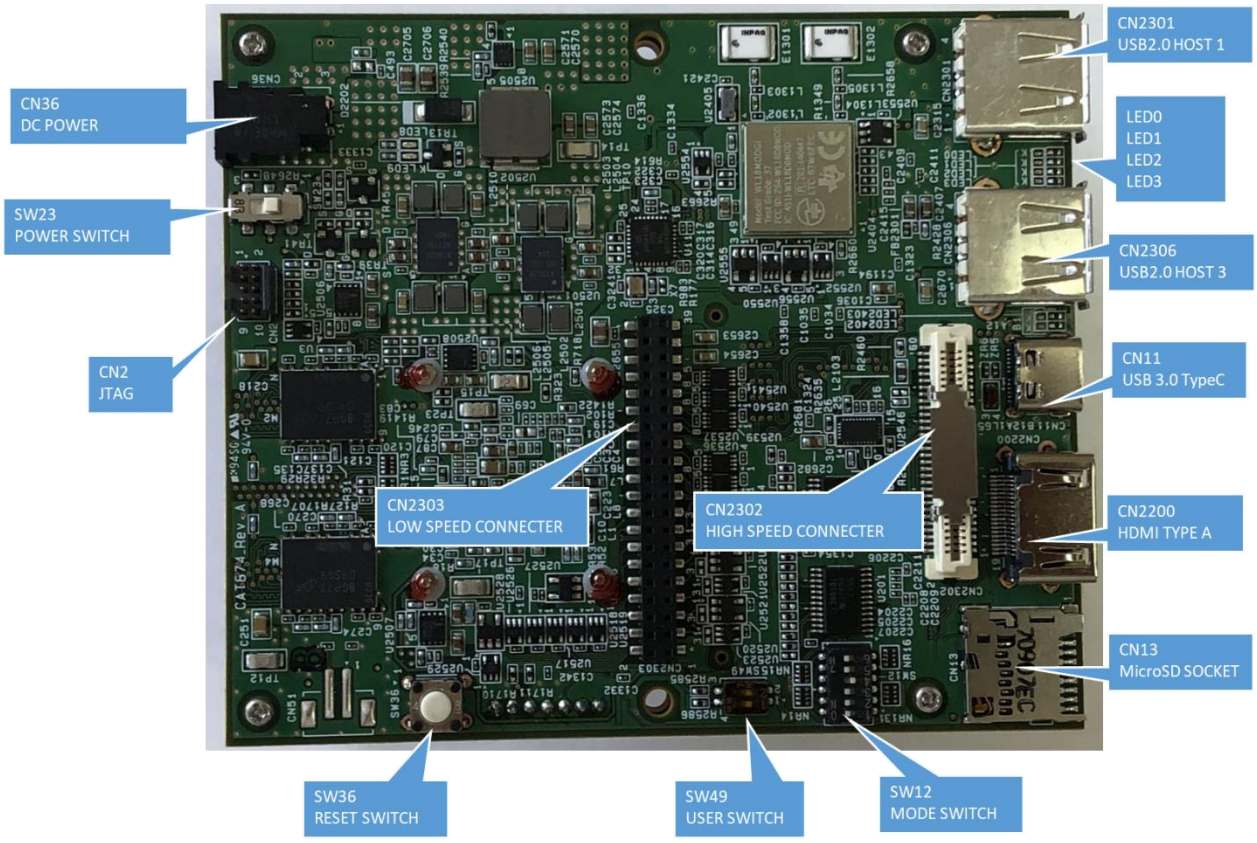
USB2.0 Type-A x2

96boards High speed connector MIPI-DSI, USB, SD

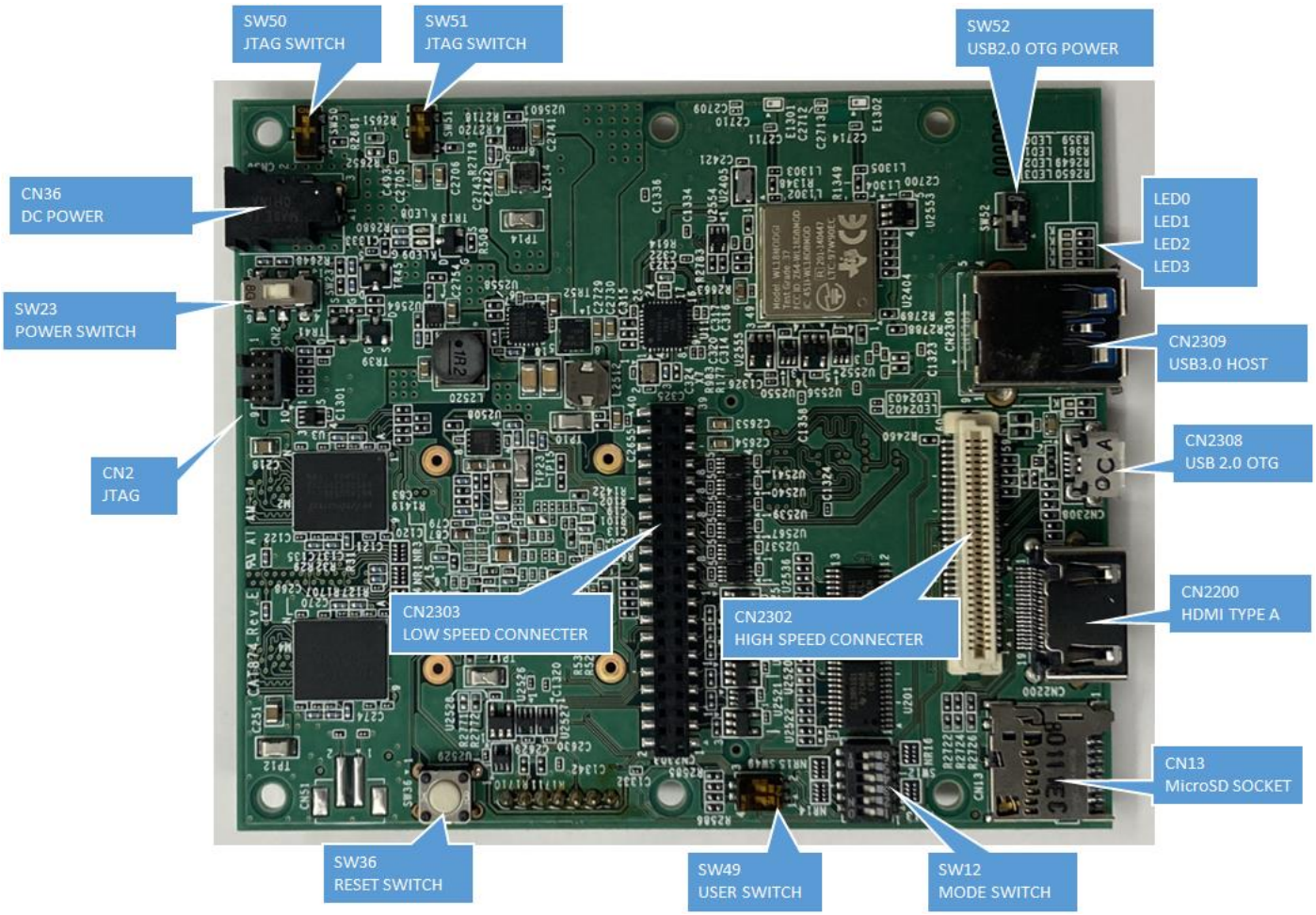
96boards Low speed connector PCM

4 Main parts arrangement 主な部品配置

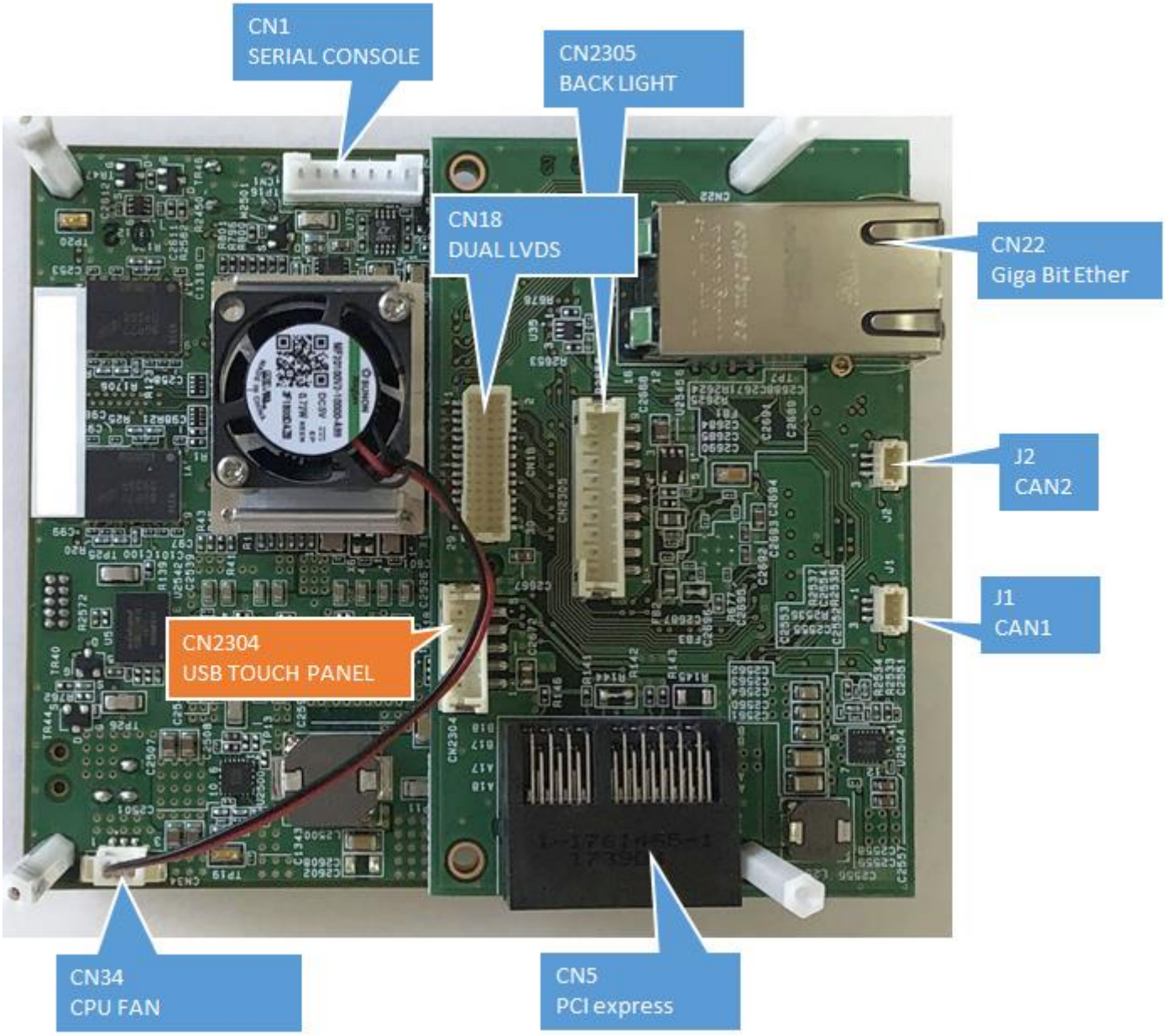
4.1 Rev.A, Rev.B, Rev.C



4.2 Rev.D, Rev. E


SW50
JTAG SWITCH
SW51
JTAG SWITCH
SW52
USB2.0 OTG POWER
CN36
DC POWER
LED0
LED1
LED2
LED3
SW23
POWER SWITCH
CN2309
USB3.0 HOST
CN2
JTAG
CN2308
USB 2.0 OTG
CN2303
LOW SPEED CONNECTER
CN2302
HIGH SPEED CONNECTER
CN2200
HDMI TYPE A
CN13
MicroSD SOCKET
SW36
RESET SWITCH
SW49
USER SWITCH
SW12
MODE SWITCH

4.3 CPU SIDE Rev.A, Rev.B, Rev.C, Rev.D, Rev.E

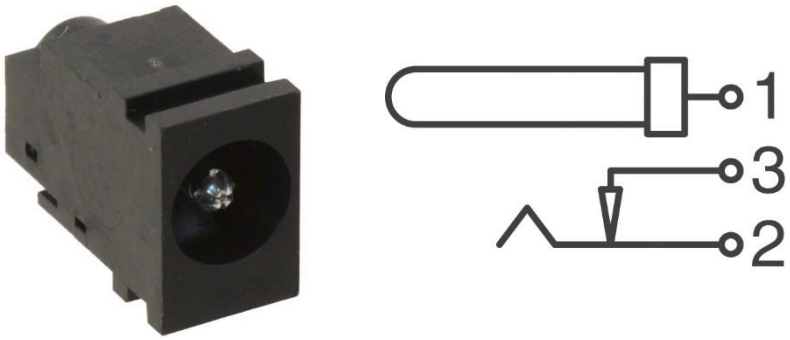


Rev.A, Rev.B, Rev.C	CN2304 USB TOUCH PANEL
Rev.D, Rev.E	CN2304 non-connect

5 Connector signal arrangement コネクタ信号配列

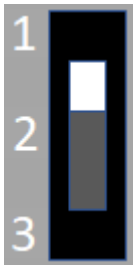
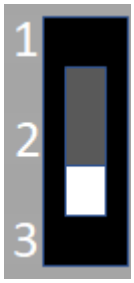
5.1 CN36 DC POWER

Part name (コネクタ形式): PJ-041H
Manufacturer (メーカー): CUI Inc.
Internal Diameter (接点内径): 1.65 mm
Outer Diameter(接点外径): 5.15 mm
Recognized Mating Diameter(嵌合相手): 1.75 x 4.75mm (EIAJ-3)



1(Center)	DC 12V In
2	GND
3	GND

5.2 SW23 POWER SWITCH

	1-2 Power off
	2-3 Power on

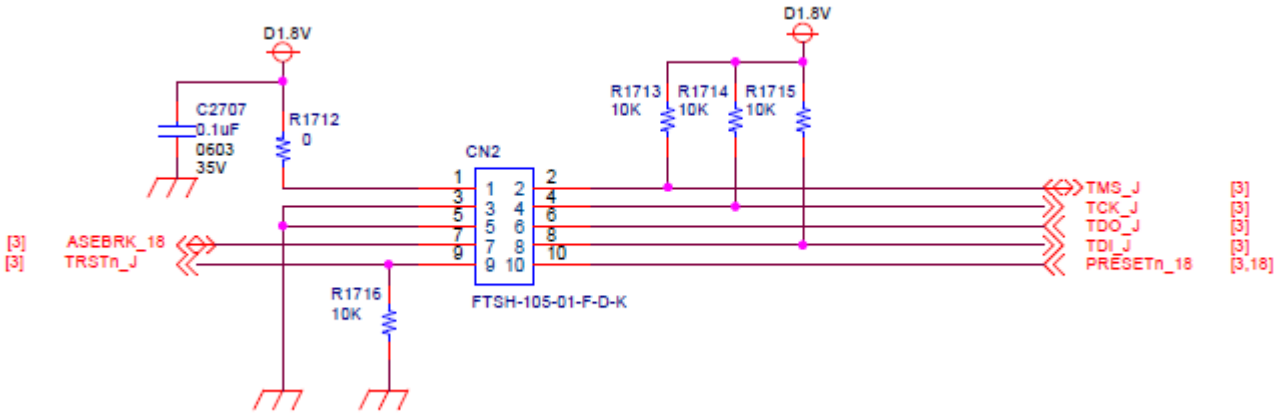
5.3 SW36 RESET SWITCH

Reset switch.See7.2 Reset system diagramfor more details.

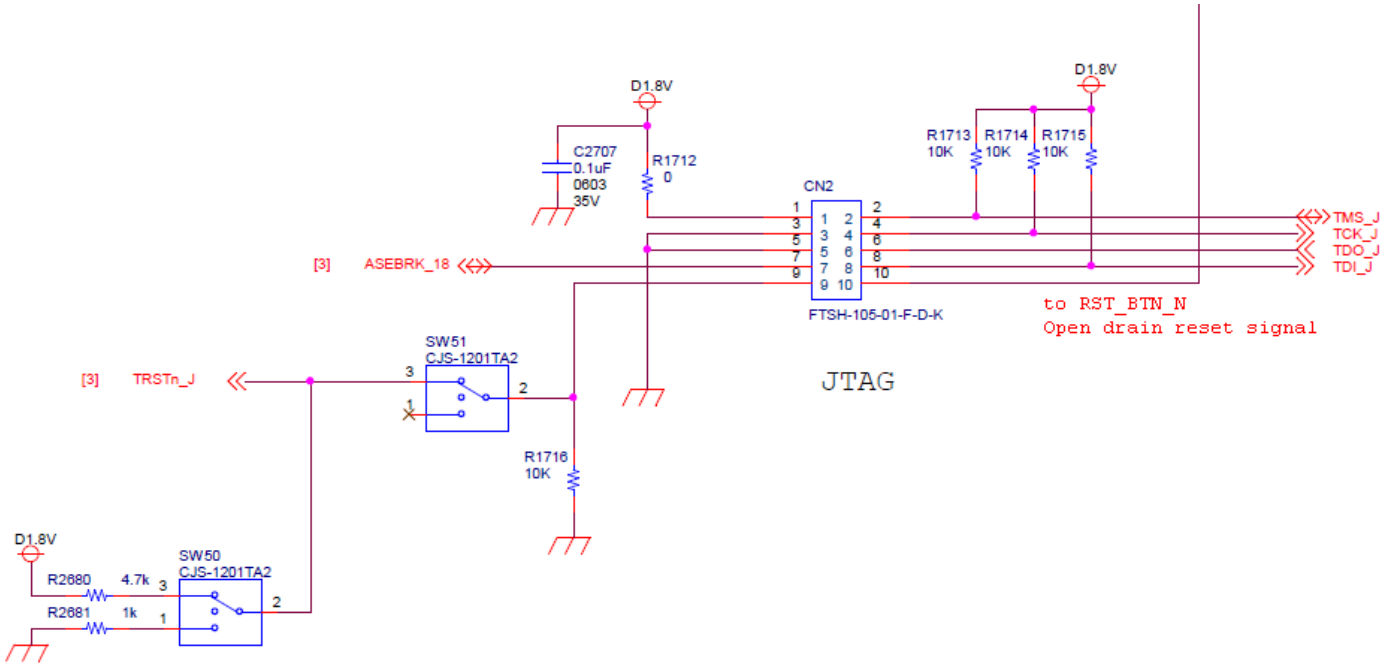
リセットスイッチ。詳細は「8.2Reset system diagram リセット系統図」 を参照してください。

5.4 CN2 JTAG

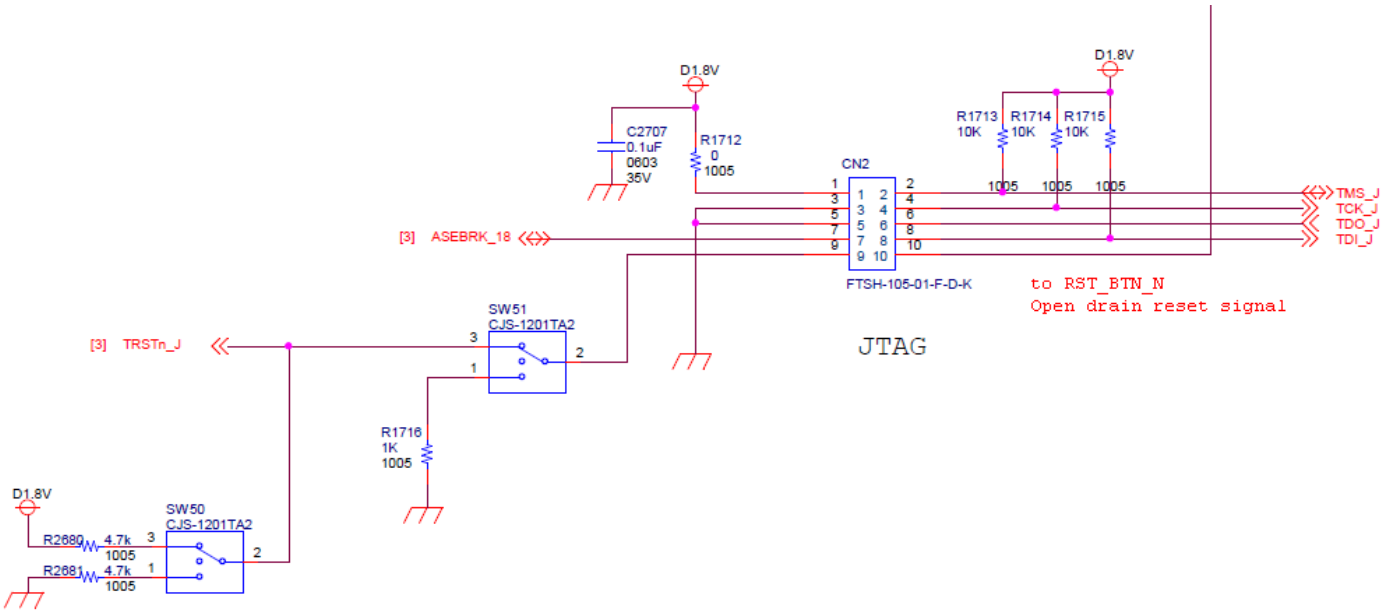
Rev.A, Rev.B



Rev.C

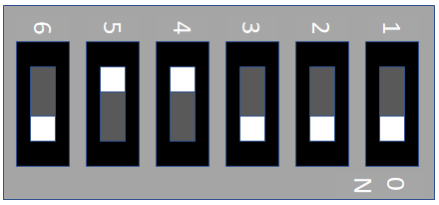


Rev.D, Rev.E



Cortex 10-pin 0.05" JTAG　Connector Pinout

The 10-pin cable is Samtec part number FFSD-05-D-12.00.01-N



JTAG mode

SW	NAME	default	
5	MD21	ON(0)	ON(0): Normal Operation　(Default) OFF(1): JTAG1 debug mode

5.5　CN2303 LOW SPEED connector

Rev.A and Rev.B

No.	96Boards Name	CAT874 (Rev.B) Name	note
1	GND	GND	
3	UART0_CTS	HRTS3#_C (L4) GP2_13	(1)
5	UART0_TxD	HRX3_C (L1) GPIO2_10	(1)
7	UART0_RxD	HTX3_C (K5) GPIO2_09	(2)
9	UART0_RTS	HCTS3#_C (L3) GP2_12	(2)
11	UART1_TxD	HRX4_B (K4) GP2_08	(2)
13	UART1_RxD	HTX4_B (K3) GP2_07	(2)
15	I2C0_SCL	SCL3 (H2)	(3)
17	I2C0_SDA	SDA3 (H3)	(3)

No.	96Boards Name	CAT874 (Rev.B) Name	note
2	GND	GND	
4	PWR_BTN_N	PWR_BTN_N_1V8	
6	RST_BTN_N	RST_BTN_N	
8	SPI0_SCLK	MSIOF0_SCK (N22)	
10	SPI0_DIN	MSIOF0_RXD (N23)	
12	SPI0_CS	MSIOF0_SYNC (N25)	
14	SPI0_DOUT	MSIOF0_TXD (N24)	
16	PCM_FS	SSI_WS349 (V22)	
18	PCM_CLK	SSI_SCK349 (V24)	

19	I2C1_SCL	SCL1 (T25)	(4)	20	PCM_DO	SSI_SDATA4 (W25)	
21	I2C1_SDA	SDA1 (T23)	(4)	22	PCM_DI	SSI_SDATA3 (V21)	
23	GPIO-A	GP1_05 (V4)		24	GPIO-B	GP1_06 (V2)	
25	GPIO-C	GP1_07 (V3)		26	GPIO-D	GP4_07 (G21)	
27	GPIO-E	GP4_08 (F23)		28	GPIO-F	GP4_09 (H21)	
29	GPIO-G	GP5_01 (P25)		30	GPIO-H	GP5_02 (P24)	
31	GPIO-I	GP5_03 (P23)		32	GPIO-J	GP5_05 (R25)	
33	GPIO-K	GP5_06 (R24)		34	GPIO-L	GP5_07 (R23)	
35	+1V8	D1.8V		36	SYS_DCIN	D12.0V	
37	+5V	D5.0V		38	SYS_DCIN	D12.0V	
39	GND	GND		40	GND	GND	

Rev.C

No.	96Boards Name	CAT874 (Rev.C) Name	note	No.	96Boards Name	CAT874 (Rev.C) Name	note
1	GND	GND		2	GND	GND	
3	UART0_CTS	HCTS3#_C (L3) GP2_12	(1)	4	PWR_BTN_N	PWR_BTN_N_1V8	
5	UART0_TxD	HTX3_C (K5) GPIO2_09	(1)	6	RST_BTN_N	RST_BTN_N	
7	UART0_RxD	HRX3_C (L1) GPIO2_10	(2)	8	SPI0_SCLK	MSIOF0_SCK (N22)	
9	UART0_RTS	HRTS3#_C (L4) GP2_13	(2)	10	SPI0_DIN	MSIOF0_RXD (N23)	
11	UART1_TxD	HTX4_B (K3) GP2_07	(2)	12	SPI0_CS	MSIOF0_SYNC (N25)	
13	UART1_RxD	HRX4_B (K4) GP2_08	(2)	14	SPI0_DOUT	MSIOF0_TXD (N24)	
15	I2C0_SCL	SCL3 (H2)	(3)	16	PCM_FS	SSI_WS349 (V22)	
17	I2C0_SDA	SDA3 (H3)	(3)	18	PCM_CLK	SSI_SCK349 (V24)	
19	I2C1_SCL	SCL1 (T25)	(4)	20	PCM_DO	SSI_SDATA4 (W25)	
21	I2C1_SDA	SDA1 (T23)	(4)	22	PCM_DI	SSI_SDATA3 (V21)	
23	GPIO-A	GP1_05 (V4)		24	GPIO-B	GP1_06 (V2)	
25	GPIO-C	GP1_07 (V3)		26	GPIO-D	GP4_07 (G21)	
27	GPIO-E	GP4_08 (F23)		28	GPIO-F	GP4_09 (H21)	
29	GPIO-G	GP5_01 (P25)		30	GPIO-H	GP5_02 (P24)	
31	GPIO-I	GP5_03 (P23)		32	GPIO-J	GP5_05 (R25)	
33	GPIO-K	GP5_06 (R24)		34	GPIO-L	GP5_07 (R23)	
35	+1V8	D1.8V		36	SYS_DCIN	D12.0V	
37	+5V	D5.0V		38	SYS_DCIN	D12.0V	
39	GND	GND		40	GND	GND	

Rev.D, Rev.E

No.	96Boards Name	CAT874 (Rev.B) Name	note	No.	96Boards Name	CAT874 (Rev.B) Name	note
1	GND	GND		2	GND	GND	
3	UART0_CTS	HRTS3#_C (L4) GP2_13	(1)	4	PWR_BTN_N	PWR_BTN_N_1V8	

5	UART0_TxD	HRX3_C (L1) GPIO1_3	(1)	6	RST_BTN_N	RST_BTN_N	
7	UART0_RxD	HTX3_C (K5) GPIO1_2	(2)	8	SPI0_SCLK	MSIOF0_SCK (N22)	
9	UART0_RTS	HCTS3#_C (L3) GP2_12	(2)	10	SPI0_DIO	MSIOF0_RXD (N23)	
11	UART1_TxD	HRX4_B (K4) GP2_8	(2)	12	SPI0_CS	MSIOF0_SYNC (N25)	
13	UART1_RxD	HTX4_B (K3) GP2_7	(2)	14	SPI0_DOUT	MSIOF0_TXD (N24)	
15	I2C0_SCL	SCL3 (H2)	(3)	16	PCM_FS	n.c.	(5)
17	I2C0_SDA	SDA3 (H3)	(3)	18	PCM_CLK	n.c.	(5)
19	I2C1_SCL	SCL1 (T25)	(4)	20	PCM_DO	n.c.	(5)
21	I2C1_SDA	SDA1 (T23)	(4)	22	PCM_DI	n.c.	(5)
23	GPIO-A	GP1_05 (V4)		24	GPIO-B	GP1_06 (V2)	
25	GPIO-C	GP1_07 (V3)		26	GPIO-D	GP4_07 (G21)	
27	GPIO-E	GP4_08 (F23)		28	GPIO-F	GP4_09 (H21)	
29	GPIO-G	GP5_01 (P25)		30	GPIO-H	GP5_02 (P24)	
31	GPIO-I	GP5_03 (P23)		32	GPIO-J	GP5_05 (R25)	
33	GPIO-K	GP5_06 (R24)		34	GPIO-L	GP5_07 (R23)	
35	+1V8	D1.8V		36	SYS_DCIN	D12.0V	
37	+5V	D5.0V		38	SYS_DCIN	D12.0V	
39	GND	GND		40	GND	GND	

Note(1) (2) CAT845 Rev. A and Rev. B Limitations.Both these revisions,TX-RX and CTS-RTS are reversed. Fiexed on Rev.C

(3) Shared with high speed connectorI2C2.

(4) Shared with high speed connectorI2C3.

(5) Rev.D　Rev.E　non-connect

注意

(1) (2) CAT845 RevA. RevB での制限事項. TX-RX および CTS-RTS が逆になっています。Rev.C で修正済み

(3) high speed connector I2C2 と共用

(4) high speed connector I2C3 と共用

(5) Rev.D,　Rev.E で未接続

5.6　CN2302 HIGH SPEED connector

Rev.A,　Rev.B,　Rev.C

No.	96Boards Name	CAT874　Name	note	No.	96Boards Name	CAT874 Name	note
1	SD_DAT0/SPI1_DOUT	SD1_DAT0 (J25)		2	CSI0_C+	CSI0_CLKP (AE13)	
3	SD_DAT1	SD1_DAT1 (J23)		4	CSI0_C-	CSI0_CLKN (AD13)	

5	SD_DAT2	SD1_DAT2 (J24)		6	GND	GND	
7	SD_DAT3/SPI1_CS	SD1_DAT3 (J22)		8	CSI0_D0+	CSI0_DATAP0 (AE15)	
9	SD_SCLK/SPI1_SCLK	SD1_CLK (H25)		10	CSI0_D0-	CSI0_DATAN0 (AD15)	
11	SD_CMD/SPI1_DIN	SD1_CMD (J21)		12	GND	GND	
13	GND	GND		14	CSI0_D1+	CSI0_DATAP1 (AC14)	
15	CLK0/CSI0_MCLK	TPU0TO0 (W22)		16	CSI0_D1-	CSI0_DATAN1 (AB14)	
17	CLK1/CSI1_MCLK	TPU0TO1 (W21)		18	GND	GND	
19	GND	GND		20	CSI0_D2+	n.c.	
21	DSI_CLK+	LT8918L _MTCP (38)		22	CSI0_D2-	n.c.	
23	DSI_CLK-	LT8918L _MTCN (39)		24	GND	GND	
25	GND	GND		26	CSI0_D3+	n.c.	
27	DSI_D0+	LT8918L _MT0P (34)		28	CSI0_D3-	n.c.	
29	DSI_D0-	LT8918L _MT0N (35)		30	GND	GND	
31	GND	GND		32	I2C2_SCL	SCL3 (H2)	(1)
33	DSI_D1+	LT8918L _MT1P (36)		34	I2C2_SDA	SDA3 (H3)	(1)
35	DSI_D1-	LT8918L _MT1N (37)		36	I2C3_SCL	SCL1 (T25)	(2)
37	GND	GND		38	I2C3_SDA	SDA1 (T23)	(2)
39	DSI_D2+	LT8918L _MT2P (40)		40	GND	GND	
41	DSI_D2-	LT8918L _MT2N (41)		42	CSI1_D0+	n.c.	
43	GND	GND		44	CSI1_D0-	n.c.	
45	DSI_D3+	LT8918L _MT3P (42)		46	GND	GND	
47	DSI_D3-	LT8918L _MT3N (43)		48	CSI1_D1+	n.c.	
49	GND	GND		50	CSI1_D1-	n.c.	
51	USB_D+	USBHUB_DM2 (26)		52	GND	GND	
53	USB_D-	USBHUB_DP2 (27)		54	CSI1_C+	n.c.	
55	GND	GND		56	CSI1_C-	n.c.	
57	HSIC_STR	n.c.		58	GND	GND	
59	HSIC_DATA	n.c.		60	RESERVED	Pull UP 4.7K to D1.8V	

Rev.D, Rev.E

No.	96Boards Name	CAT874 Name	note
1	SD_DAT0/SPI1_DOUT	n.c.	(3)
3	SD_DAT1	n.c.	(3)
5	SD_DAT2	n.c.	(3)
7	SD_DAT3/SPI1_CS	n.c.	(3)
9	SD_SCLK/SPI1_SCLK	n.c.	(3)

No.	96Boards Name	CAT874 Name	note
2	CSI0_C+	CSI0_CLKP (AE13)	
4	CSI0_C-	CSI0_CLKN (AD13)	
6	GND	GND	
8	CSI0_D0+	CSI0_DATAP0 (AE15)	
10	CSI0_D0-	CSI0_DATAN0 (AD15)	

11	SD_CMD/SPI1_DIN	n.c.	(3)	12	GND	GND	
13	GND	GND		14	CSI0_D1+	CSI0_DATAP1 (AC14)	
15	CLK0/CSI0_MCLK	TPU0TO0 (W22)		16	CSI0_D1-	CSI0_DATAN1 (AB14)	
17	CLK1/CSI1_MCLK	TPU0TO1 (W21)		18	GND	GND	
19	GND	GND		20	CSI0_D2+	n.c.	
21	DSI_CLK+	n.c.	(3)	22	CSI0_D2-	n.c.	
23	DSI_CLK-	n.c.	(3)	24	GND	GND	
25	GND	GND		26	CSI0_D3+	n.c.	
27	DSI_D0+	n.c.	(3)	28	CSI0_D3-	n.c.	
29	DSI_D0-	n.c.	(3)	30	GND	GND	
31	GND	GND		32	I2C2_SCL	SCL3 (H2)	(1)
33	DSI_D1+	n.c.	(3)	34	I2C2_SDA	SDA3 (H3)	(1)
35	DSI_D1-	n.c.	(3)	36	I2C3_SCL	SCL1 (T25)	(2)
37	GND	GND		38	I2C3_SDA	SDA1 (T23)	(2)
39	DSI_D2+	n.c.	(3)	40	GND	GND	
41	DSI_D2-	n.c.	(3)	42	CSI1_D0+	n.c.	
43	GND	GND		44	CSI1_D0-	n.c.	
45	DSI_D3+	n.c.	(3)	46	GND	GND	
47	DSI_D3-	n.c.	(3)	48	CSI1_D1+	n.c.	
49	GND	GND		50	CSI1_D1-	n.c.	
51	USB_D+	n.c.	(3)	52	GND	GND	
53	USB_D-	n.c.	(3)	54	CSI1_C+	n.c.	
55	GND	GND		56	CSI1_C-	n.c.	
57	HSIC_STR	n.c.		58	GND	GND	
59	HSIC_DATA	n.c.		60	RESERVED	Pull UP 4.7K to D1.8V	

Note

(1) Shared withlow speed connector I2C0. Low speed connector I2C0 と共用

(2) Shared withlow speed connector I2C1. Low speed connector I2C1 と共用

(3) Rev.D, Rev.E SD, DSI, USB are non-connect

Rev.D, Rev.E SD, DSI, USB は未接続

5.7 CN2301 CN2306 USB2.0 Host connector

Rev.A, Rev.B, Rev.C only

Connected to RZ/G2E CPU through USB2.0 hub LSI “uPD720115K8-711-BAK-A”.

usb hub ic uPD720115K8-711-BAK-A を通して RZ/G2E CPU と接続されています。

5.8 CN2308 USB 2.0 OTG

Rev.D, Rev.E only

Connected to RZ/G2E CPU USB2.0

RZ/G2E CPU の USB2.0 と接続されています。

5.9 CN11 USB3.0 Host connector

Rev.A, Rev.B, Rev.C only

Connected to RZ/G2E CPU USB3.0.

RZ/G2E CPU の USB3.0 と接続されています。

5.10 CN2309 USB 3.0 Host connector

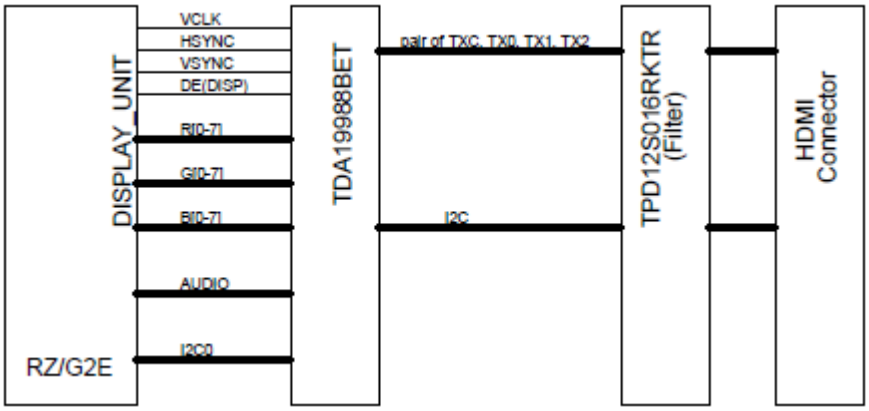
Rev.D, Rev.E only

Connected to RZ/G2E CPU USB3.0.

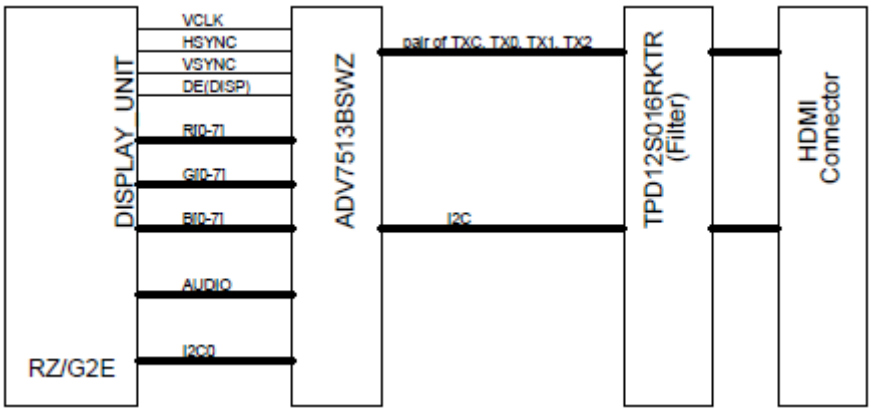
RZ/G2E CPU の USB3.0 と接続されています。

5.11 CN2200 HDMI type A

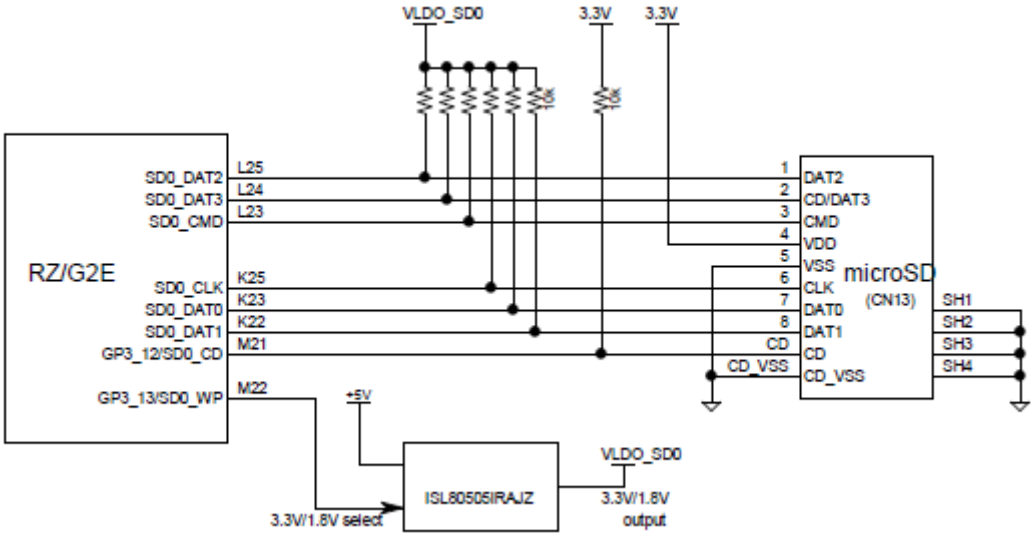
Rev.A, Rev.B, Rev.C



Rev.D, Rev.E



5.12 CN13 microSD

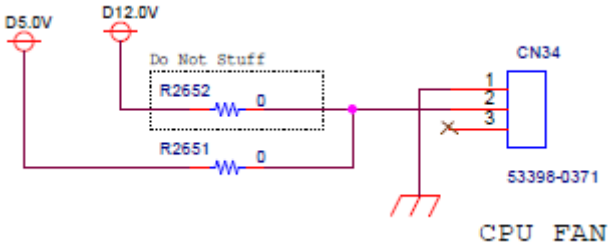


5.13 CN1 SERIAL CONSOLE

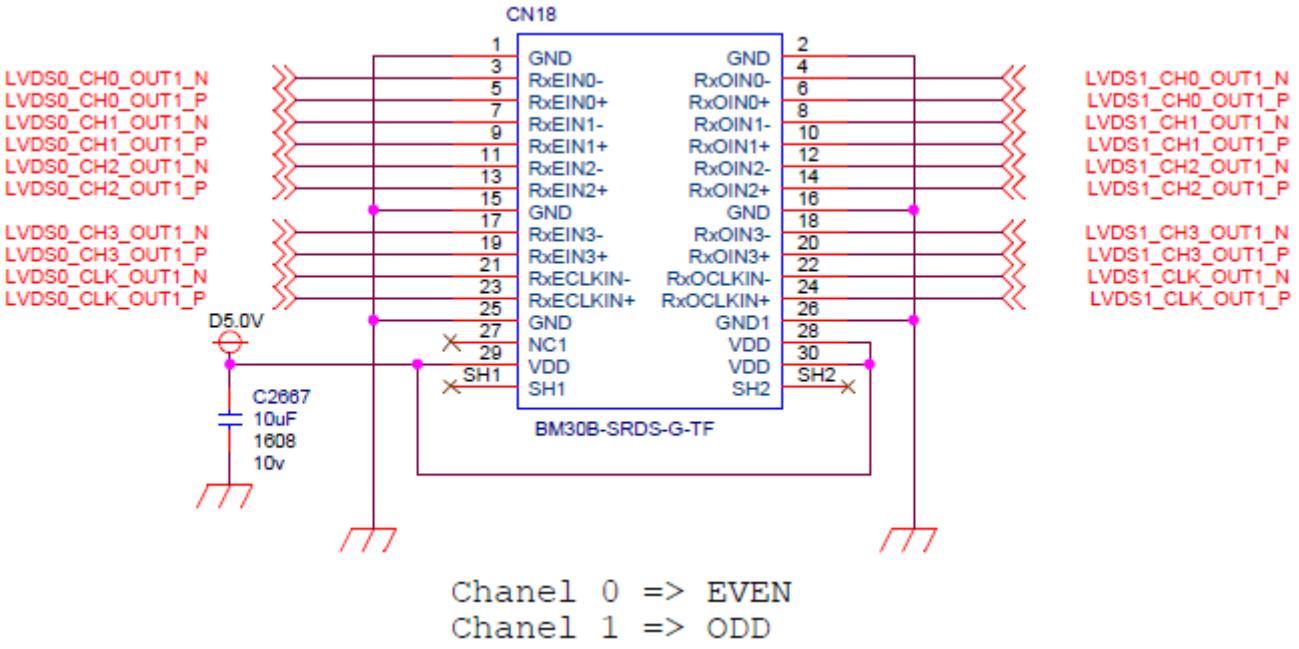
1	**GND**
2	**SCIF2_RXD (3.3V)**
3	**SCIF2_TXD (3.3V)**
4	GND
5	RESET_IN
6	V_BAT (RTC　backup battery)
7	GND

Connect to the PC using the supplied micro USB conversion cable. baud rate is 115200.
付属の micro USB 変換ケーブルを用いで PC と接続してください。baudrate 115200。

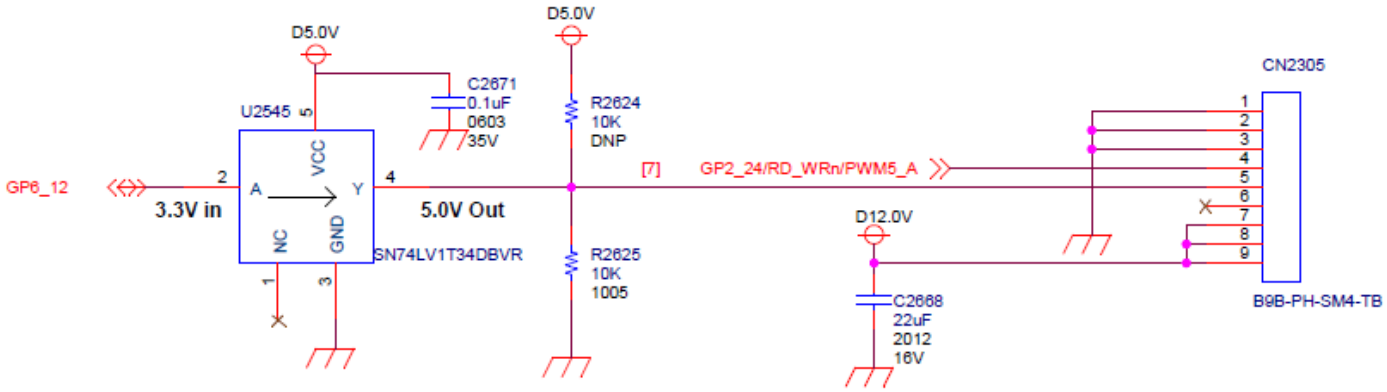
5.14 CN34 CPU FAN



5.15 CN18 DUAL LVDS

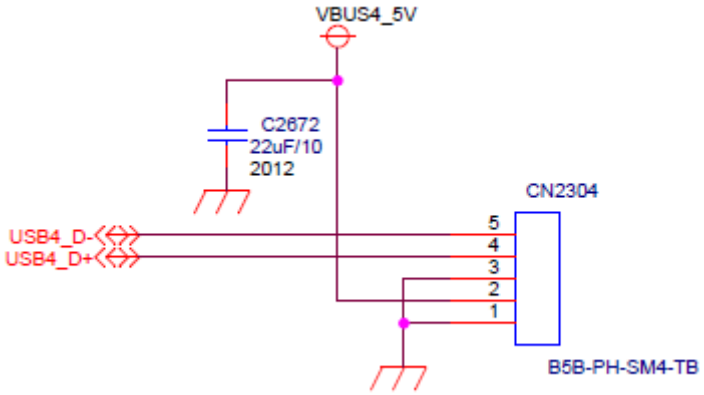


5.16 CN2305 LCD backlight

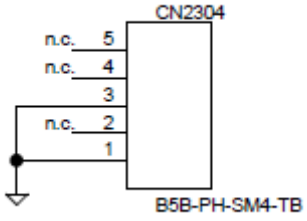


5.17 CN2304 USB touchpanel

Rev.A, Rev.B, Rev.C



Rev.D,　Rev.E

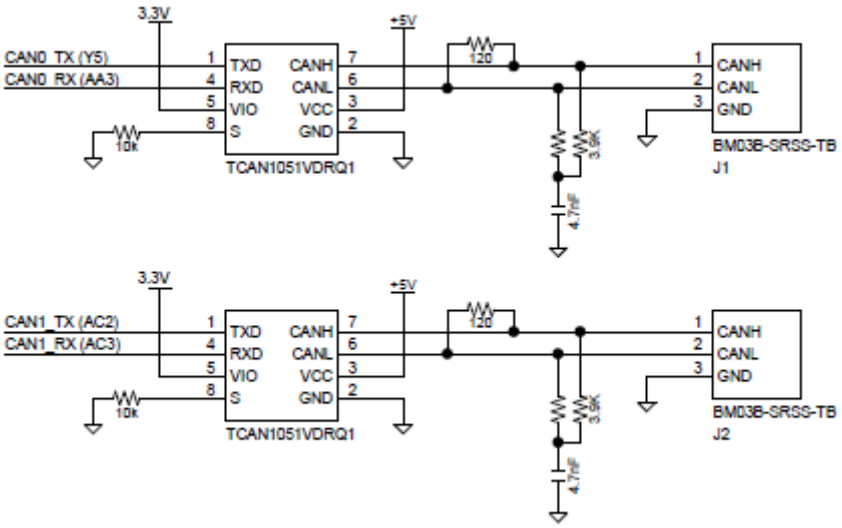


5.18　CN22 Gigabit Ether

5.19　CN5 PCI express

JTAG, SMCLK, SMDAT not support.

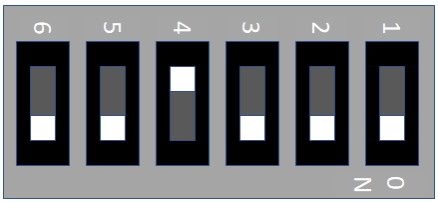
5.20　J1 J2 CAN



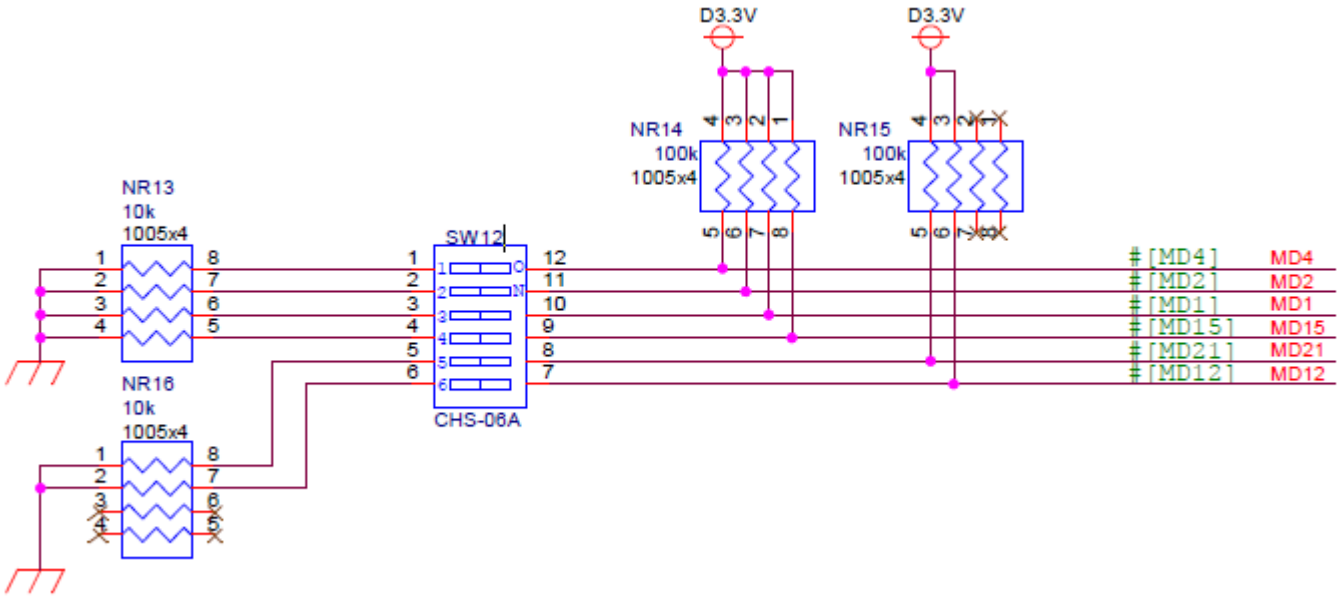
6 Switch スイッチ

6.1 SW12 MODE SWITCH

Factory Dafault (QSPI boot mode)
出荷時状態



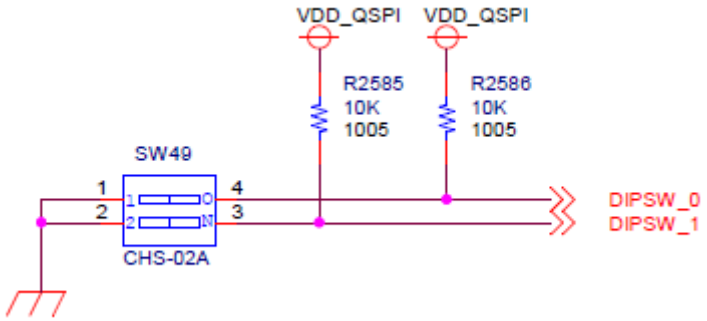
SW12 (default)



The logic becomes 0 by turning on the SW. The logic becomes 1 by turning off the SW.
SW を ON にすることで論理 0 になります。 SW を OFF にすることで論理 1 になります。

SW	NAME	default	
1	MD4	ON(0)	MD[4,2,1] select boot mode. MD3 fiexed to 1.
2	MD2	ON(0)	MD[4,3,2,1]
3	MD1	ON(0)	0100 QSPI ROM boot at single read 40 MHz using DMA (default) 1110 USB download mode 1111 SCIF download mode
4	MD15	OFF(1)	ON(0): AArch32 OFF(1):AArch64 (default)
5	MD21	ON(0)	ON(0): Normal Operation (default) OFF(1): JTAG1 debug mode
6	MD12	ON(0)	ON(0): Turning SSCG off (default) OFF(1) : Turning SSCG on. [Spread Spectrum Clock Generator]

6.2 SW49 USER SWITCH



The logic becomes 0 by turning on the SW. The logic becomes 1 by turning off the SW. User can use.

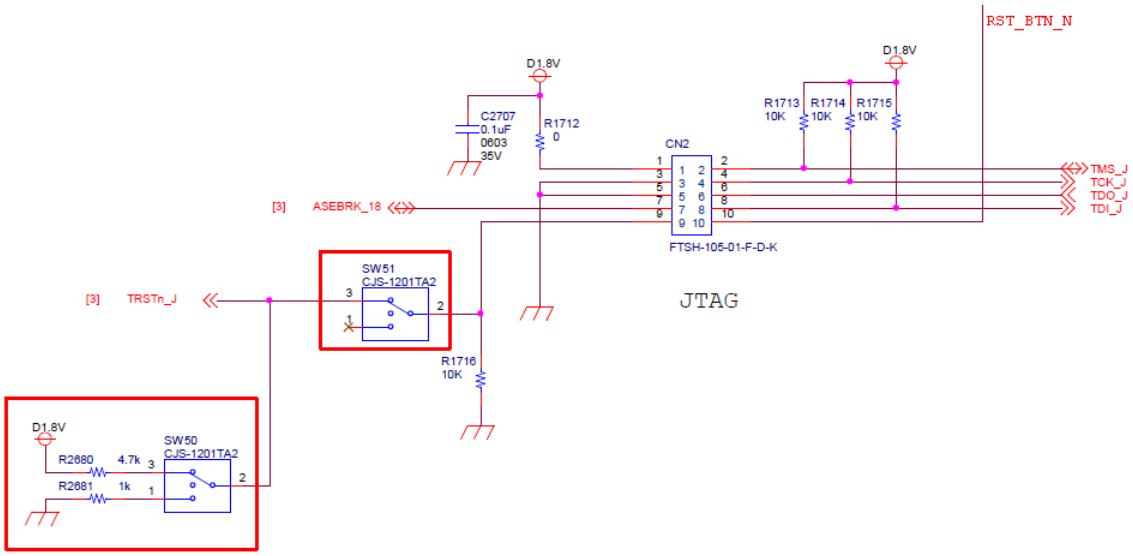
SW を ON にすることで論理 0 になります。 SW を OFF にすることで論理 1 になります。ユーザ・アプリケーションで使用できます。

	CPU pin name	GPIO PIN	Logic
DIPSW_0	QSPI1_SPCLK (K1)	GP2_06	ON=0, OFF=1
DIPSW_1	QSPI1_SSL (L2)	GP2_11	ON=0, OFF=1

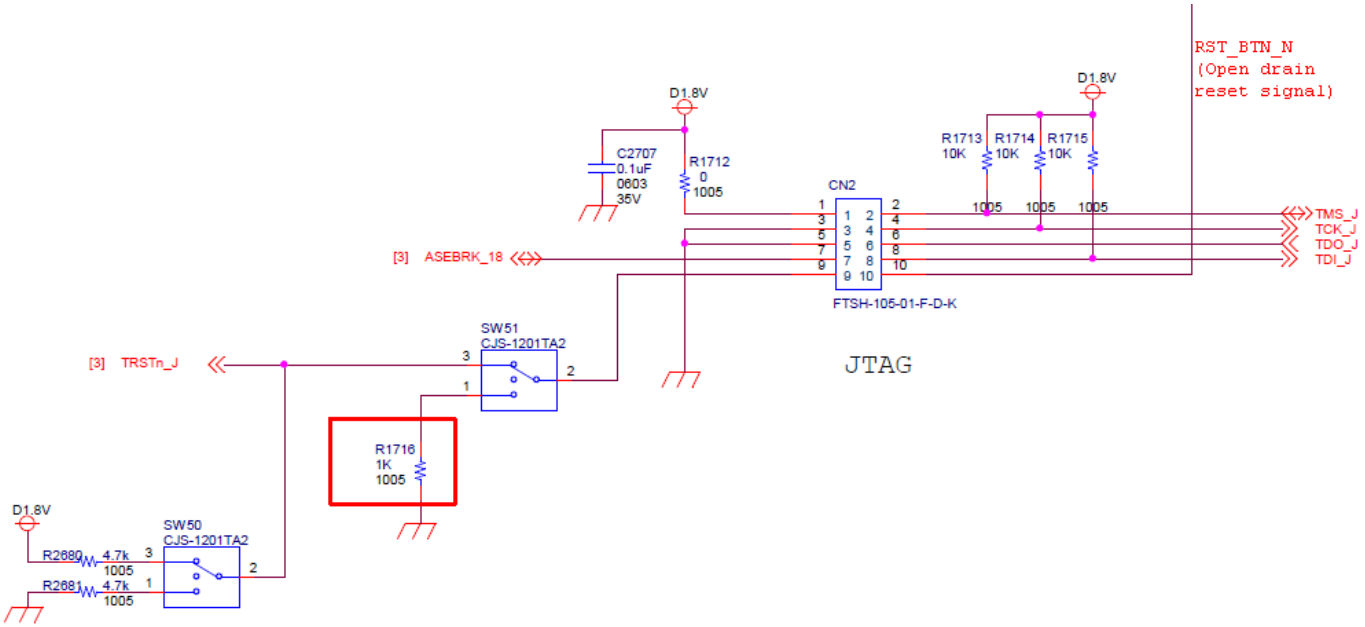
6.3 SW50, SW51 JTAG nRESET

Rev.C and later only. Rev.C 以降のみ
CN2 (JTAG) pin9 RZ/G2E TRSTn_J

Rev.A, Rev.B, Rev.C

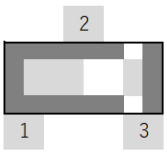


Rev.D, Rev.E



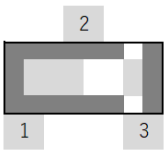
SW51	CN2 (JTAG) Pin9	
2-3 (Default)	Connect to TRSTn_J	for KMC Partner-JET2
1-2	Disconnect with TRSTn_J and Pull Down	other JTAGs

Part. Name　CJS-1200TA　(nidec-copal-electronics)



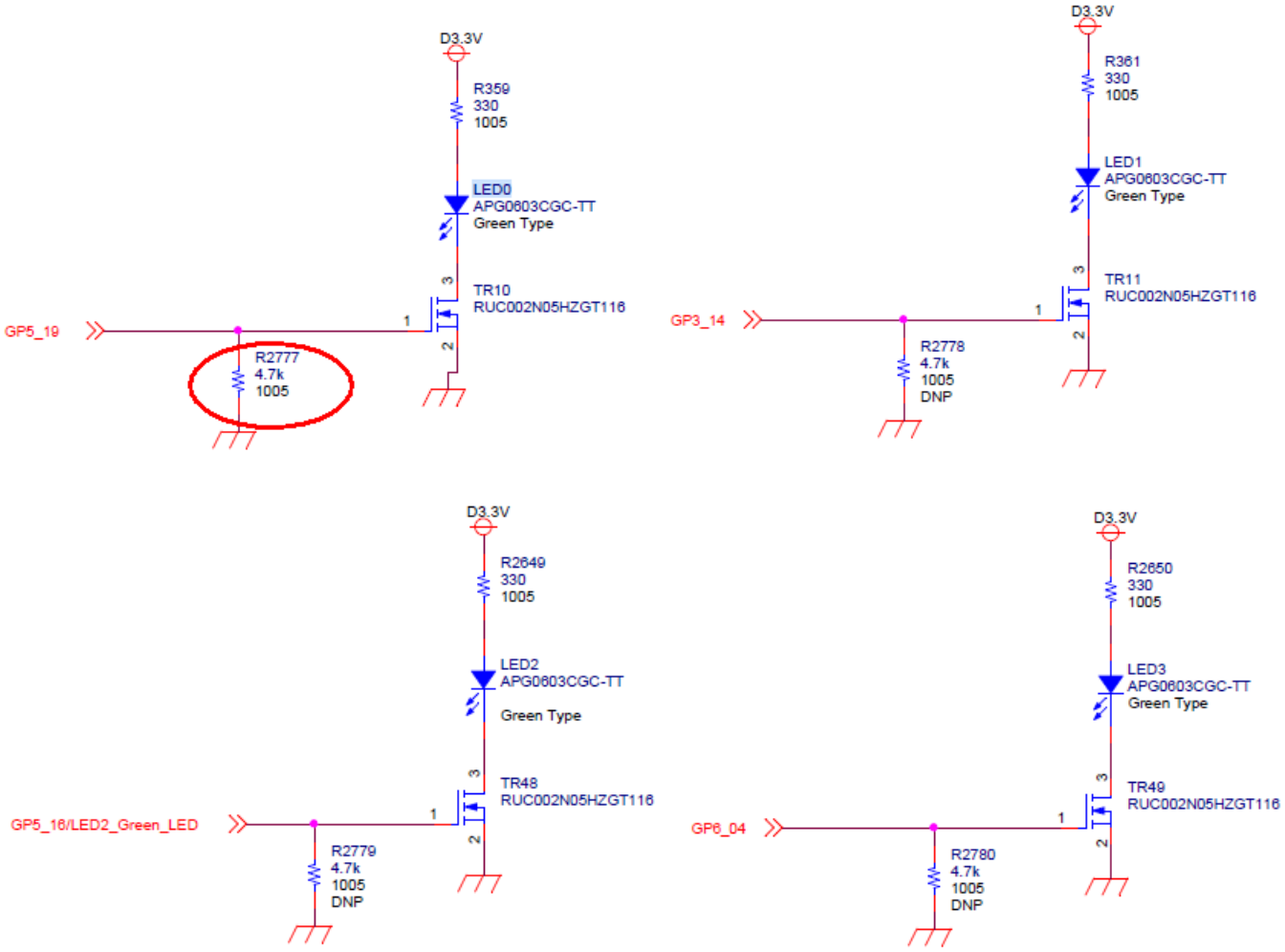
SW50	RZ/G2E TRSTn_J	
2-3 (Default)	Pull UP D1.8V	other JTAGs
1-2	Pull Down	for KMC Partner-JET2

Part. Name　CJS-1200TA　(nidec-copal-electronics)



7 LED

	GPIO_PIN	Color	Logic
LED0	GP5_19	Green	ON=1
LED1	GP3_14	Green	ON=1
LED2	GP4_10 Rev.A, Rev.B, Rev.C GP5_16 Rev.D, Rev.E	Green	ON=1
LED3	GP6_04	Green	ON=1



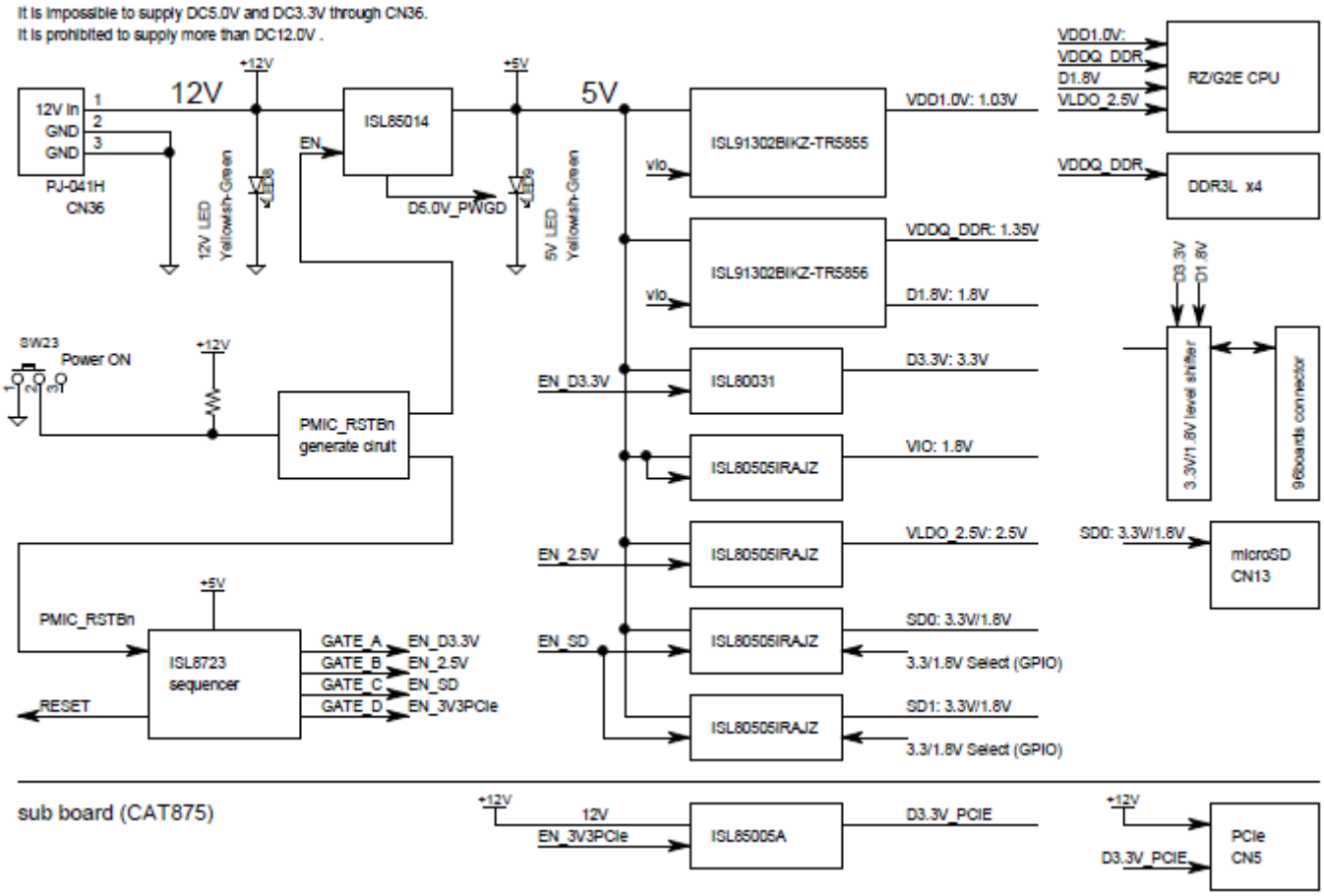
Revision Detect

	LED0 GP5_19	LED1 GP3_14	LED2 GP5_16	LED3 GP6_04
Rev.A, Rev.B, Rev.C	--	--	--	--
Rev.D, Rev.E	Pull Down 4.7K	--	--	--

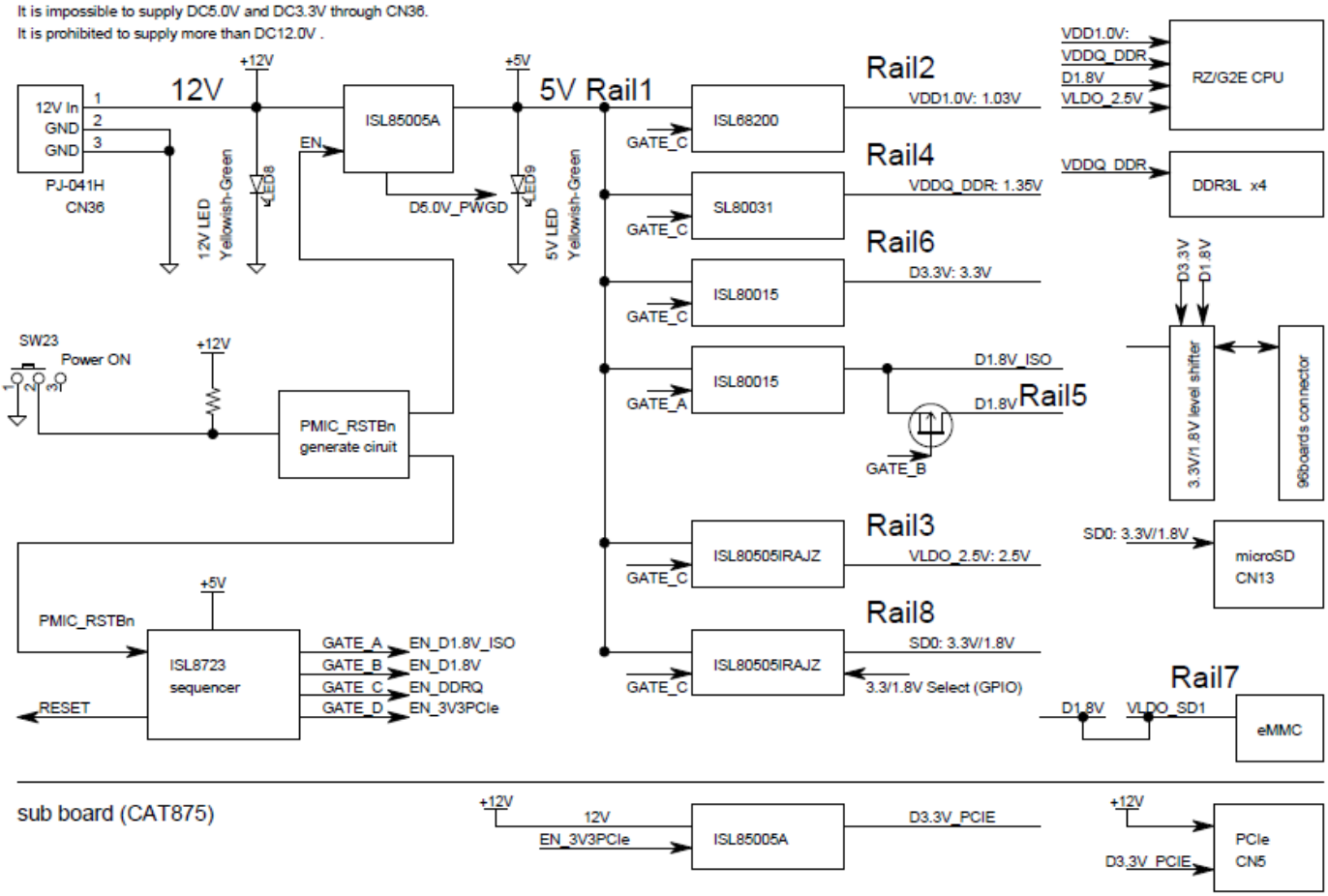
8　Power supply and reset system diagram 電源、リセット系統図

8.1　Power supply diagram 電源系統図

Rev.A,　Rev.B,　Rev.C

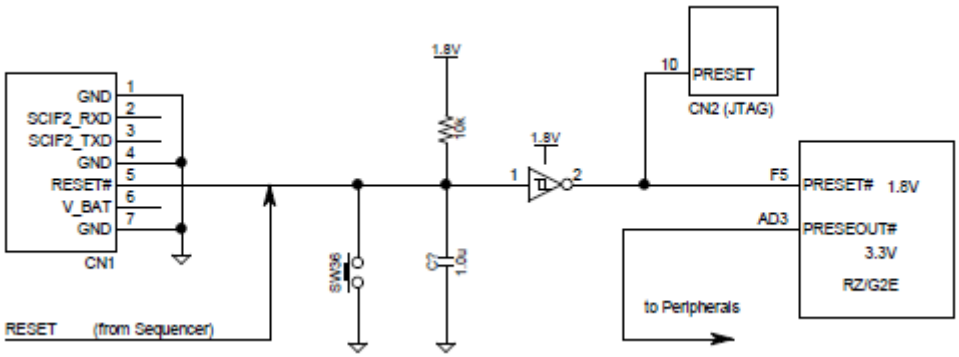


Rev.D,　Rev.E



8.2 Reset system diagram リセット系統図

Rev.A, Rev.B



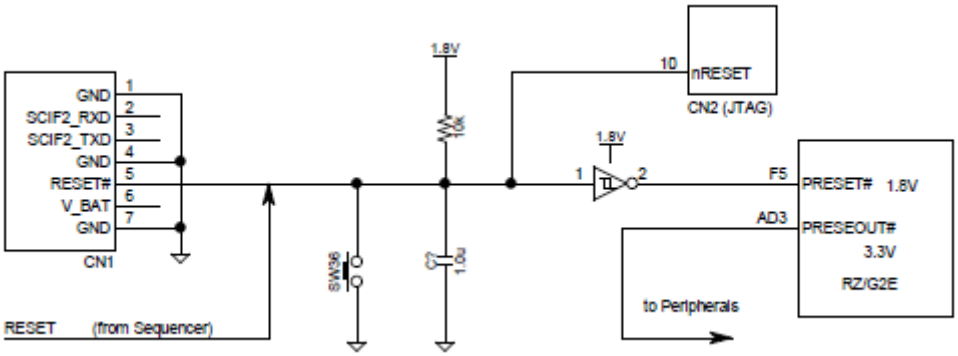
Cautions specific to CAT 874 (Rev. A, Rev, B).
CN2 JTAG connector 10pin nRESET is connected tobuffer output IC. Therefore, do not use the reset input from the JTAG 10 pin. Connect to CN1-5 pin RESET # with an open collector.

CAT874 (Rev.A, Rev,B) 注意点

CN2 JTAG コネクタ 10pin の PRESETn-18 が バッファ出力 IC と接続されています。従いまして JTAG

10pin からのリセット入力は使用しないでください。 CN1- 5 ピン RESET# に接続してください。

Rev.C, Rev.D, Rev.E



9 Booting Linux Linux の起動までの手順

9.1 Writing image file to microSD.

Download microSD image files from “si-linux.co.jp”download site.There are threeimage files to download.
弊社ダウンロードサイトから microSD イメージを取得してください。３種類のイメージファイルを用意しています。

```
http://download.si-linux.co.jp/cat874/sdimage/
    user: cat874user
    pass: 874catuser
```

filename	microSD Size		
cat874_bsp_sdimage_1G_{date}.bin.gz	1G byte	core-image-bsp	Minimal tools
cat874_hmidemo_sdimage_2G_{date}.bin.gz	2G byte	core-image-hmi	Graphical Demo
cat874_debian9_sdimage_4G_{date}.bin.gz	4G byte	debian9 arm64	Debian9

{date} part is date datafilled bybelow rule “yyyymmdd”. Get a latest file.
{date}部分は日付となります。一番新しいファイルを取得してください。

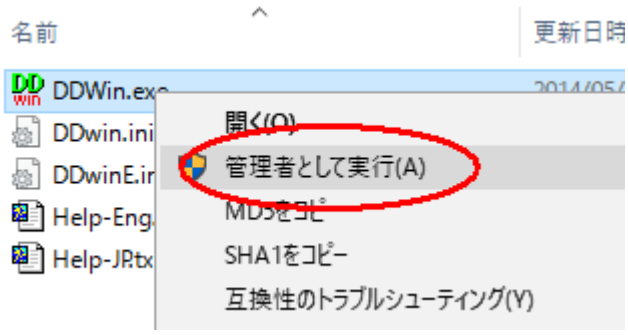
unzip .gz images. and write it into your microSD by ‘Win32 Disk imager’ or ‘dd for windows’.
.gz ファイルの圧縮を展開したあとに、Win32 Disk imager や dd for windows を使って microSD イメージファイルを microSD に書き込んでください。

win32 disk Imager

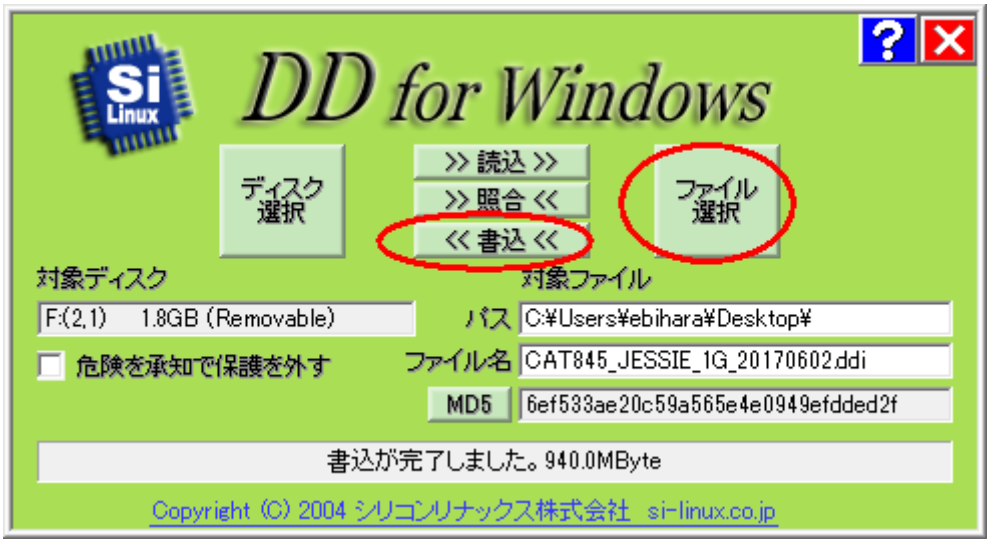
```
https://sourceforge.net/projects/win32diskimager/
```

dd for windows

```
http://www.si-linux.co.jp/techinfo/index.php?DD%20for%20Windows
```



Whenusing “dd for windows”you mustboot this programas Administrator.Some errorwill cause, but just OK and go forward.
dd for windows は 右クリック＞管理者として実行を選び実行してください。
サイズが合わないなどの警告が出ますが OK を押します。



When using 4GBsize microSD,and writingimage file, there will be 2 partition(p1, p2).

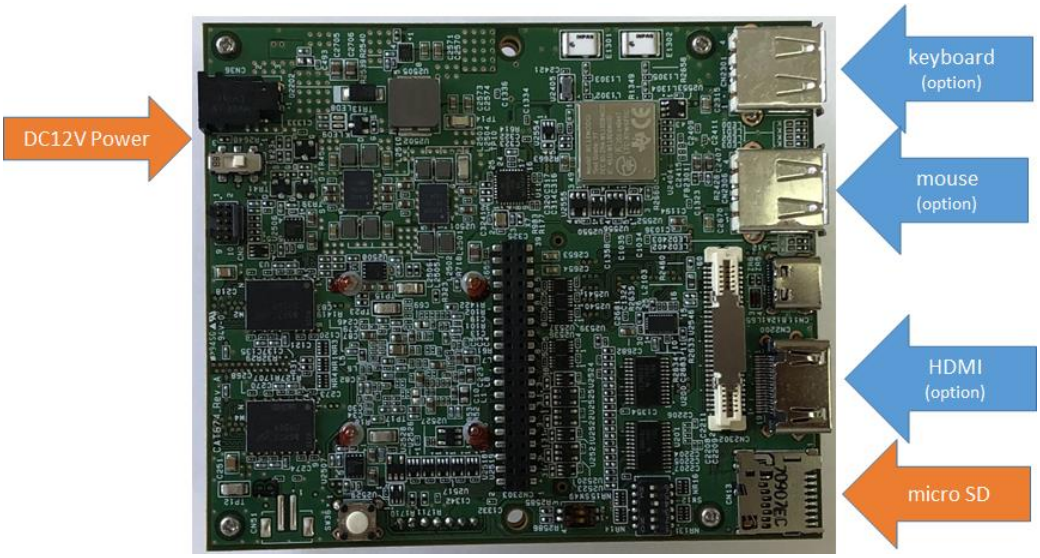
4G バイトの microSD へイメージを書き込んだ場合、次のように 2 つのパーティション(p1, p2)ができます。

```
    Device       Boot       Start       End   Sectors    Size  Id Type
>>  /dev/sda1                2048    133119    131072     64M   e W95 FAT16 (LBA)
    /dev/sda2              133120   1981439   1848320  902.5M  83 Linux
    Free space            1982464   7774207   5791744    2.8G
```

968 Mbyte of microSD is used. Remainingareais recognizedas unusedarea.

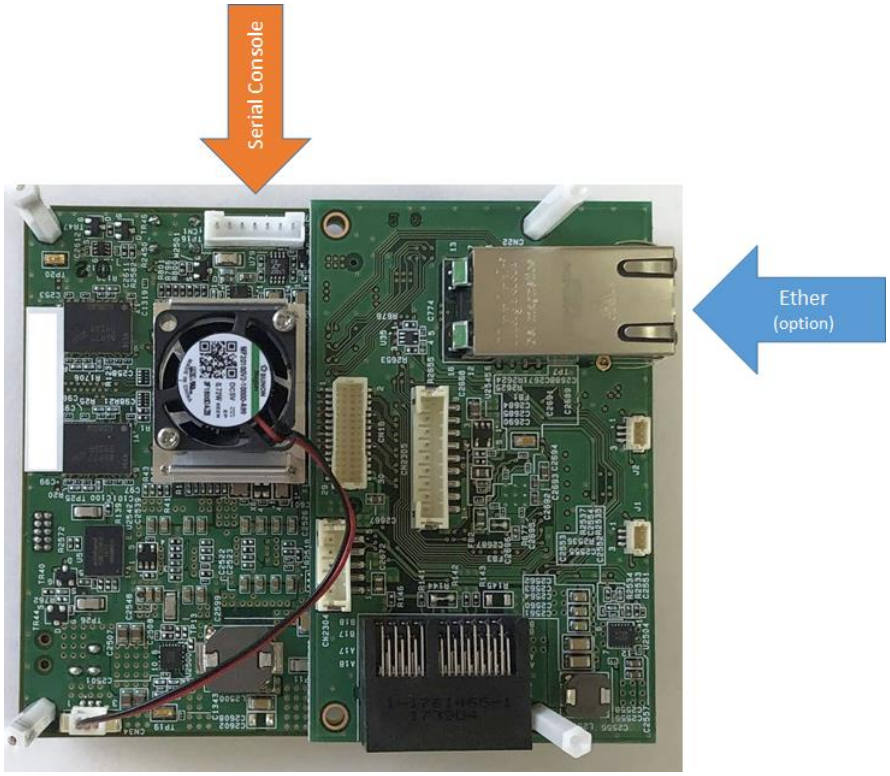
microSD のうち前半 968Mbyte が使われています。後半は未使用で空いています。

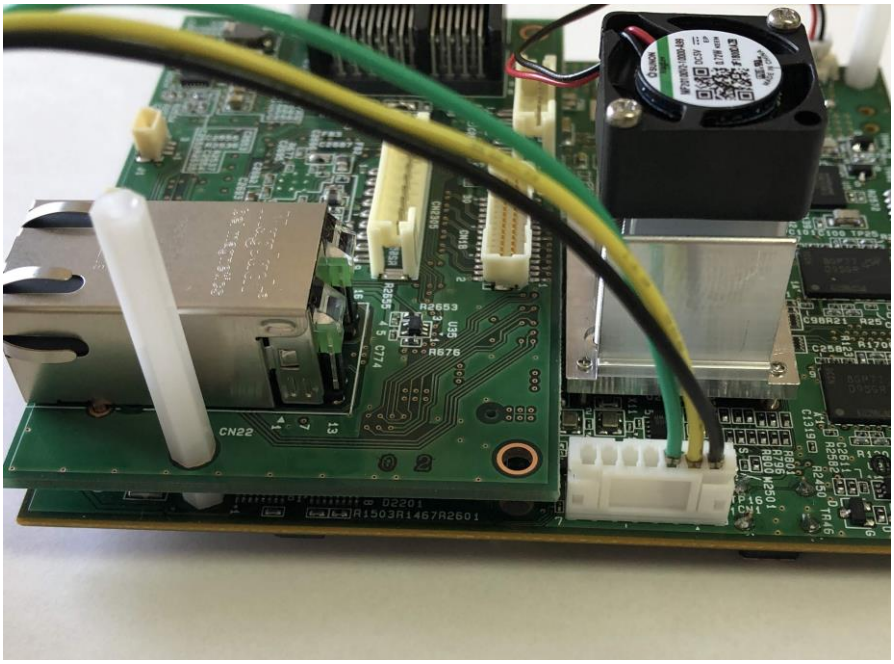
9.2 CAT874 setting and power ON



Insert the completed microSD into the CN13 socket.

書き込み完了した microSD を CN13 ソケットに挿入します。



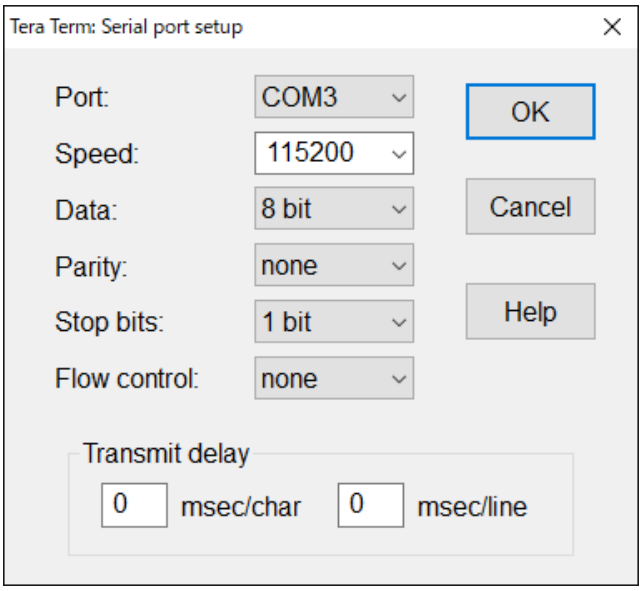


Connect serial microUSB conversion cable to CN1. When using a 5pin cable, use 1, 2, 3 pins according to the 1 pin side

付属のシリアル-microUSB 変換ケーブルを CN1 に接続します。5pin ケーブルを使う場合は 1pin 側に合わせ、1,2,3pin を使用します。

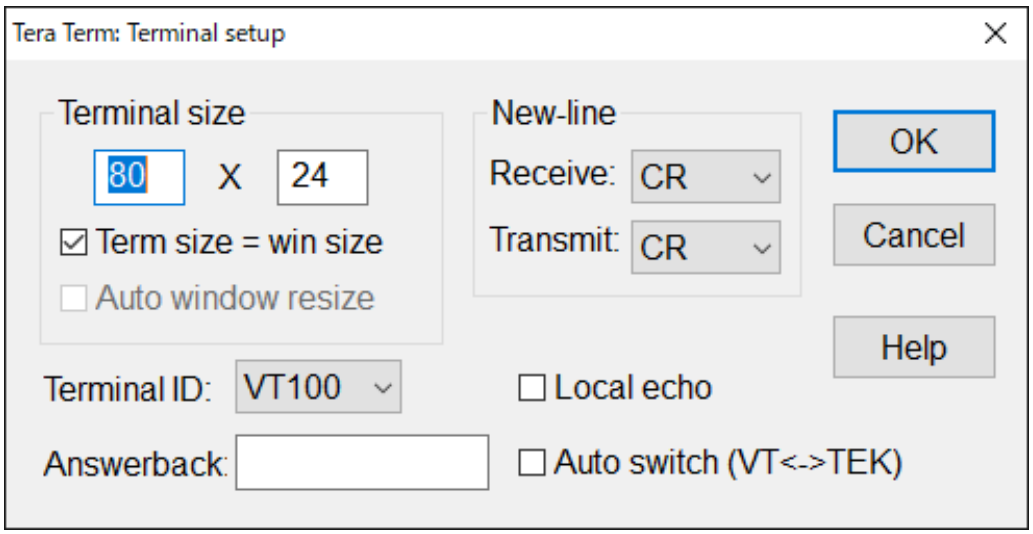
Communication using terminal software.(Case when using TeraTerm)
通信端末ソフトの設定　(TeraTerm を使う例)

Setup > Serial port…
設定＞シリアルポート




```
Speed: 115200 bps
Data: 8bit
Parity: None
Stop bit: 1bit
Flow control: None
```

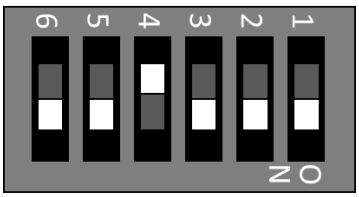
Setup > Terminal…
設定＞端末



改行コードを CR とします。
Make sureline feed code is set to CR.

9.3 Booting u-boot

Turn off the power and set DIPSW to the following state (factory default)
電源を切り DIPSW を次の状態します（出荷時状態）



6	5	4	3	2	1
ON	ON	OFF	ON	ON	ON

Following message willdisplayed when power is turned on.
Press any key during the countdown of “3, 2, 1,,, “ displayedat the u-boot command prompt.

電源を入れると次のメッセージが表示されます。3,2,1,,, のカウントダウンの間になにかキーを押し、u-boot のコマンドプロンプトを表示させます。

CAT874 Rev.A and Rev.B

```
U-Boot 2018.09 (Apr 14 2019 - 23:21:25 +0000)

CPU: Renesas Electronics R8A774C0 rev 1.0
Model: Silicon Linux EK874 RZ/G2E board
DRAM:  896 MiB
Bank #0: 0x048000000 - 0x07fffffff, 896 MiB

MMC:   sd@ee100000: 0
Loading Environment from SPI Flash... SF: Detected w25m512jv with page size 256 Bytes, erase size 4 KiB,
 total 32 MiB
OK
In:    serial@e6e88000
Out:   serial@e6e88000
Err:   serial@e6e88000
Net:
Error: ethernet@e6800000 address not set.
eth-1: ethernet@e6800000
Hit any key to stop autoboot:  0
```

CAT874 Rev.C

```
U-Boot 2018.09 (Dec 09 2019 - 08:01:25 +0000)

CPU: Renesas Electronics R8A774C0 rev 1.1
Model: Silicon Linux EK874 RZ/G2E board
DRAM:  1.9 GiB
Bank #0: 0x048000000 - 0x0bfffffff, 1.9 GiB
```

```
MMC:   sd@ee100000: 0
Loading Environment from SPI Flash... SF: Detected w25q512jv with page size 256 Bytes, erase size 4 KiB,
 total 64 MiB
OK
In:    serial@e6e88000
Out:   serial@e6e88000
Err:   serial@e6e88000
Net:   eth0: ethernet@e6800000
Hit any key to stop autoboot:  0
```

9.4 Setting Linux startup parameters

Insert microSD, turn the poweron, and type the following commandin uboot.
microSD を挿入して電源を入れ、uboot で以下のコマンドをタイプします。

=> Indicates uboot prompt. There is no need to type.
=> は uboot のプロンプトを示します。タイプする必要はありません。

```
=> setenv bootargs 'root=/dev/mmcblk0p2 rootwait ro'
=> setenv bootcmd 'fatload mmc 0:1 0x48080000 Image; fatload mmc 0:1 0x48000000 Image-r8a774c0-ek874.dtb
; booti 0x48080000 - 0x48000000'
=> saveenv
=> reset
```

9.5 Login to Linux

When “login:” is displayed, you can login using “root” for username (no password).
login: が表示されたら root （パスワードなし）でログインできます。

```
Poky (Yocto Project Reference Distro) 2.4.3 ek874 ttySC0

ek874 login: root
```

When updated to cat874_debian9_sdimage_4G_{date}.bin, following user “kaihatsu” will be registered.
cat874_debian9_sdimage_4G_{date}.bin を書き込んだ場合、次のユーザが登録されています。

User ID	Password
root	root
kaihatsu	kaihatsu

10 Peripherals

10.1 GPIO

RZ/G2E GPIO PIN	Linux GPIO Base
GP0_xx	494 + xx
GP1_xx	471 + xx
GP2_xx	445 + xx
GP3_xx	429 + xx
GP4_xx	418 + xx
GP5_xx	398 + xx
GP6_xx	380 + xx

```
LED0     GP5_19   (398 + 19)  => gpio417
LED1     GP3_14   (429 + 14)  => gpio443
LED2     GP4_10   (418 + 10)  => gpio428
LED3     GP6_04   (380 + 4)   => gpio384
```

```
DIPSW_0  GP2_06   (445 + 6)   => gpio451
DIPSW_1  GP2_11   (445 + 11)  => gpio456
```

```
# echo 417 > /sys/class/gpio/export                          # request gpio417
# echo out > /sys/class/gpio/gpio417/direction               # set gpio417 (GP5_19) output
# echo 1 > /sys/class/gpio/gpio417/value                     # turn ON LED0
# echo 0 > /sys/class/gpio/gpio417/value                     # turn OFF LED0
```

10.2 UART

RZ/G2E UART	Base address	CAT874	Linux
scif2	0xe6e88000	Console (CN1)	/dev/ttySC0
hscif2	0xe6560000	Bluetoth WL1837MODGI	/dev/ttySC1
hscif3	0xe66a0000	96 low speed connector UART0	/dev/ttySC2
hscif4	0xe66b0000	96 low speed connector UART1	/dev/ttySC3

```
# stty -F /dev/ttySC2 115200
# echo “hello” > /dev/ttySC2                    # write test
# cat /dev/ttySC2                               # read test

(ctrl+c) to stop this process. (ctrl+c) を押して終了する
```

11 Additional Information

Additional information can be found at below URL.
追加サポート情報はこちら

```
http://www.si-linux.co.jp/catwiki/index.php?CAT874
```